CLAIM 1 IS CANCELED.

2. (Amended) The method of Claim 45 wherein in said providing step (b) said vertical width of said n-type dopant region is less than about 2000 Å.

3. (Amended) The method of Claim 2 wherein in said providing step (b) said vertical width of said n-type dopant region is from about 800 to about 1200 Å.

4. (Amended) The method of Claim 45 wherein in said providing step (b) said n-type dopant region has a peak doping concentration and said collector has a peak doping concentration, wherein said peak doping concentration of said n-type dopant region is greater than said peak doping concentration of said collector.

5. (Amended) The method of Claim 45 wherein in said providing step (c) said base has a peak doping concentration and wherein said n-type dopant region has a peak doping concentration that is lower than said peak doping concentration of said base.

6. (Amended) The method of Claim 45 wherein in said providing step (b) said n-type dopant region comprises a dopant selected from the group consisting of As, Sb and P.

7. The method of Claim 6 wherein said dopant is Sb.

8. (Amended) The method of Claim 6 wherein in said providing step (b) said n-type dopant region is formed by ion implantation and activation annealing.

9. The method of Claim 8 wherein said ion implantation is performed at an ion dose of from about 2E11 to about 1E13 cm^{-2} and at an energy of from about 20 to about 150 keV.

10. The method of Claim 9 wherein said ion implantation is performed at an ion dose of from about 5E11 to about 5E12 cm^{-2} and at an energy of from about 30 to about 50 keV.

11. The method of Claim 8 wherein said activation annealing is performed at a temperature of about 900°C or higher for about 15 seconds or less.

12. (Amended) The method of Claim 45 wherein in said forming step (c) said n-type dopant region is located adjacent the base-collector junction.

13. (Amended) The method of Claim 45 wherein in said forming step (c) further comprises providing a lightly doped collector separating said n-type dopant region from said base.

14. The method of Claim 13 wherein in said forming step (c) said lightly doped collector has a vertical width of about 1000 to about 3000 Å.

15. (Amended) The method of Claim 45 wherein said forming step (c) comprises forming a heterojunction.

16. The method of Claim 15 wherein in said step of forming a heterojunction comprises depositing a SiGe-containing layer on said collector, said SiGe-containing layer comprising a polycrystalline region abutting a single-crystal region.

17. The method of Claim 16 wherein said forming step (d) includes forming a patterned insulator on said SiGe-containing layer, wherein said patterned insulator includes an opening that exposes a portion of said single-crystal region, and forming an emitter polysilicon on said patterned insulator and in said opening.

18. The method of Claim 17 wherein said step of forming a patterned insulator on said SiGe-containing layer comprises lithography and etching.

19. The method of Claim 16 wherein portions of said single-crystal region are doped so as to form extrinsic base regions therein.

20. The method of Claim 16 wherein said SiGe-containing layer comprises SiGeC.

21. The method of Claim 16 wherein said step of depositing a SiGe-containing layer is performed using a low-temperature deposition process selected from the group consisting of chemical vapor deposition (CVD), plasma-assisted CVD, atomic layer deposition (ALD), chemical solution deposition and ultra-high vacuum CVD.

22. (Amended) The method of Claim 45 wherein said deep collector is formed by ion implantation and annealing.

23. (Amended) The method of Claim 45 wherein in said providing step (a) said sub-collector is formed by ion implantation into a substrate or by epitaxially growing said sub-collector on a substrate.

24. (Amended) A bipolar transistor comprising:

an emitter, a base, a collector, a base-emitter junction, and a base-collector junction, wherein said collector comprises a subcollector, a deep collector and a n-type dopant region between said sub-collector and said base-collector junction, said n-type dopant region is located atop and in contact with said deep collector and has a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage and a dopant concentration sufficiently high to restrict base widening when the base-junction is forward biased.

25. (Amended) The bipolar transistor of Claim 24 wherein said n-type dopant region is located adjacent the base-collector junction.

26. (Amended) The bipolar transistor of Claim 24 wherein said vertical width of said n-type dopant region is less than about 2000 Å.

27. (Amended) The bipolar transistor of Claim 26 wherein said vertical width of said n-type dopant region is from about 800 to about 1200 Å.

28. (Amended) The bipolar transistor of Claim 24 wherein said n-type dopant region has a peak doping concentration and said collector has a peak doping concentration, wherein said peak doping concentration of said n-type dopant region is greater than said peak doping concentration of said collector.

29. (Amended) The bipolar transistor of Claim 24 wherein said base has a peak doping concentration and wherein said n-type dopant region has a peak doping concentration that is lower than said peak doping concentration of said base.

30. (Amended) The bipolar transistor of Claim 24 wherein said n-type dopant region comprises a dopant selected from the group consisting of As, Sb and P.

31. The bipolar transistor of Claim 30 wherein said dopant is Sb.

32. (Amended) The bipolar transistor of Claim 24 further comprising a lightly doped collector separating said n-type dopant region from said base.

33. The bipolar transistor of Claim 32 wherein said lightly doped collector has a vertical width of about 1000 to about 3000 Å.

34. (Amended) The bipolar transistor of Claim 24 wherein said n-type dopant region provides a higher speed of the transistor by restricting base widening.

35. The bipolar transistor of Claim 24 wherein said sub-collector is on a semiconductor substrate.

36. The bipolar transistor of Claim 35 wherein said semiconductor substrate is a semiconducting material selected from the group consisting of Si, Ge, SiGe, GaAs, InAs, InP, Si/Si, Si/SiGe and silicon-on-insulators.

37. (Amended) The bipolar transistor of Claim 24 wherein said n-type dopant region has a dopant concentration of from about 5E16 to about 5E17 cm^{-3}.

38. (Amended) The bipolar transistor of Claim 24 wherein said n-type dopant region has a dopant concentration of from about 8E16 to about 2E17 cm^{-3}.

39. The bipolar transistor of Claim 24 wherein the transistor comprises a heterojunction.

40. The bipolar transistor of Claim 39 wherein said heterojunction comprises a SiGe-containing base layer on a silicon substrate.

41. The bipolar transistor of Claim 40 wherein said SiGe-containing base layer comprises a polycrystalline region abutting a single-crystal region.

42. The bipolar transistor of Claim 41, wherein said emitter comprises polycrystalline silicon contacting a portion of said single-crystal region through an opening in a patterned insulator.

43. The bipolar transistor of Claim 41 wherein said single-crystal region includes extrinsic and intrinsic base regions.

44. The bipolar transistor of Claim 40 wherein said SiGe-containing base layer comprises SiGeC.

--45. A method of fabricating a bipolar device comprising the steps of:

(a) providing a structure comprising at least a sub-collector region, a collector region and isolation regions, said collector region including a deep collector region located therein;

(b) forming a n-type dopant region within said collector region so as to be in contact with said deep collector, said n-type dopant region having a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage and a dopant concentration sufficiently high to restrict base widening when a base-emitter junction is forwarded biased;

(c) forming a base; and

(d) forming an emitter.--